Fundamentals of Electric Drives 2nd edition El Sharkawi Solutions Manual

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Chapter 2:
Introduction to Solid State Devices

Problem 2.1:

A bipolar transistor is connected to a resistive load as shown in Figure 2.21. The source voltage $V_{CC} = 60$ V and $R_L = 5\ \Omega$.

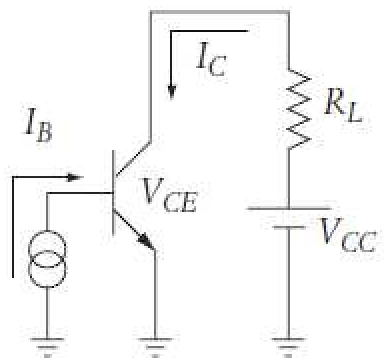


Figure 2.21

In the saturation region, the collector-emitter voltage $V_{CE} = 5$ V and $\beta = 6$.

While the transistor is in the saturation region, calculate the following:

a. Load current
b. Load power
c. Losses in the collector circuit
d. Losses in the base circuit
e. Efficiency of the circuit

Solution:

a. Load current:

$I_L = (V_{CC} - V_{CE})/R_L = (60 - 5)/5$
$= 11$ A

b. Load power:

$P_L = I_L * V_L = I_L * I_L * R_L = 605$ W

c. Losses in the collector circuit:

$P_{LossCollector} = V_{CE} * I_C$
$= V_{CE} * I_L$ (Since $I_C = I_L$)
$= 5 * 11 = 55$ W

d. Losses in the base circuit:

$$P_{LossBase} = I_B * V_{BE} = \frac{I_C}{\beta} * V_{BE} = \frac{11}{6} * 0.7 = 1.283W$$

e. Total Efficiency of the circuit = Total Useful Power/Total Power Input

$= 605/(605 + 55 + 1.283)$
$= 91.489\%$

Problem 2.2:

For the transistor in Problem 2.1, compute the load current, load power, and the efficiency of the circuit when the transistor is in the cutoff region. Assume that the collector current is 100 mA in the cutoff region.

Solution:

Cutoff region $I_C = 100$ mA
Therefore, $I_{load} = I_c = 100$ mA
Load Power $= I^2_{load}*R_L = 0.01*5 = 0.05$ W

$$\text{Efficiency of the circuit} = \frac{P_{load}}{P_{in}} = \frac{0.05}{60*0.1} = 0.833\%$$

Problem 2.3:

Design a snubbing circuit for a power bipolar transistor that operates in a circuit between a resistive load of 20 Ω and an ac source of 120 V (rms), 60 Hz. The available ratings of the transistor are

$$\left(\frac{dv_{ce}}{dt}\right)_{\max} = 300\ \text{V}/\mu\text{sec}$$

$$\left(\frac{di_c}{dt}\right)_{\max} = 20\ \text{A}/\mu\text{sec}$$

$$\left(V_{ce}\right)_{\max} = 600\ \text{V}$$

Solution:

Designing the snubbing circuit:

$$\frac{dV_{scr}}{dt} = 300\ \text{V}/\mu\text{s}$$

$$\frac{di_{scr}}{dt} = 20\ \text{A}/\mu\text{s}$$

$$R = 20\ \Omega$$

$$(V_{ce})_{\max} = 600\ \text{V}$$

Assuming a 50% factor of safety design,

$$0.5*\left[\frac{di_1}{dt}\right]_{\max} = \frac{V_{CEmax}}{R^2 * C}$$

$$0.5*\left[\frac{dV}{dt}\right]_{\max} = V_{CEmax} * \frac{R}{L}$$

Therefore,

$$Ls = 80 \text{ mH}$$

$$Cs = 0.15\ \mu\text{F}$$

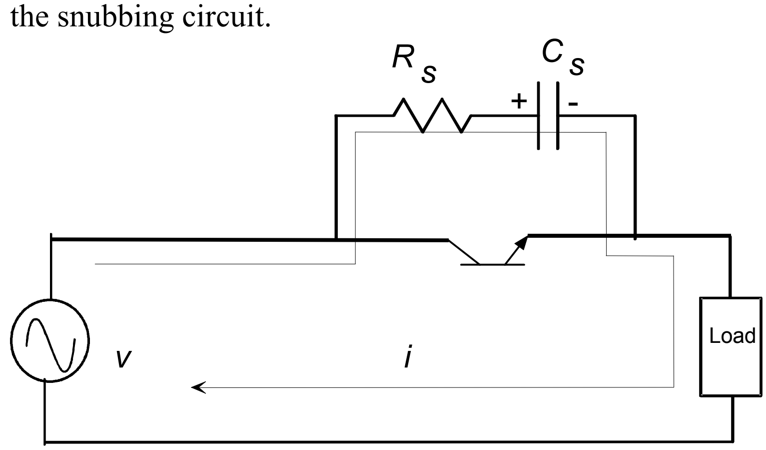
Problem 2.4:

Design a snubbing circuit for a power transistor that operates in a circuit consisting of an inductive load and an ac source. The resistive component of the load is 20 Ω and the inductive component is 10 Ω. The ac source is 120 V (rms) at 60 Hz. The transistor has the same ratings as the one in Problem 2.3.

Solution**:**

Because of the large load inductance, there is no need for additional snubbing inductance.

Examine the circuit in the figure. When the transistor opens, the current flow in the snubbing circuit.



Designing the snubbing circuit:

$$\frac{dV_{scr}}{dt} = 300 \text{ V/}\mu\text{s}$$

$$\frac{di_{scr}}{dt} = 20 \text{ A/}\mu\text{s}$$

$$R = 20\ \Omega$$

$$(V_{ce})_{\max} = 600 \text{ V}$$

$$L_l = \frac{10}{2\pi 60} = 26.53 \text{ mH}$$

Assuming a 50% factor of safety design and assuming a standard value of capacitor of $C_s = 1.0\ \mu F$
Use the equations below:

$$0.5 * \left[\frac{di_1}{dt}\right]_{\max} = \frac{V_{CEmax}}{(R_L + R_S)^2 * C}$$

$$0.5 * \left[\frac{dV}{dt}\right]_{\max} = V_{CEmax} * \frac{(R_S + R_L)}{L}$$

Therefore,

$$Ls = 240 - 26.53 = 213.47 \text{ mH}$$

$$Cs = 0.10\ \mu\text{F}$$

$$Rs = 60 - 20 = 40\ \Omega$$